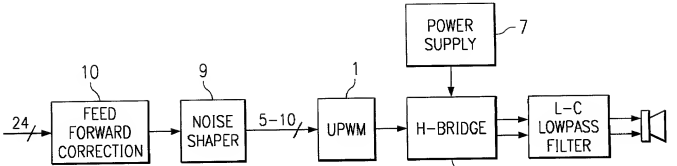



FIG. 1

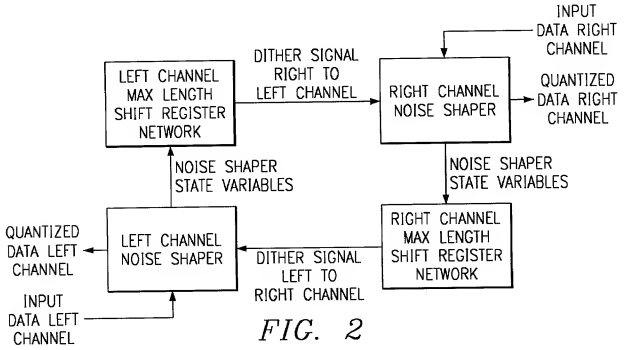



FIG. 2

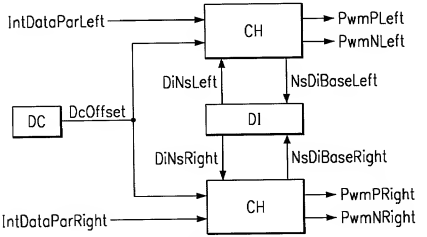



FIG. 3

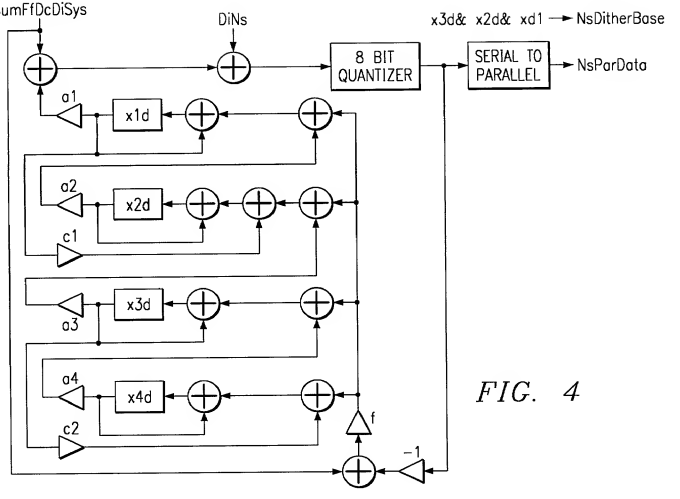

SumFfDcDiSys
DiNs
x3d& x2d& xd1
NsDitherBase
8 BIT QUANTIZER
SERIAL TO PARALLEL
NsParData
a1
x1d
a2
x2d
c1
x3d
a3
a4
x4d
c2
f
-1

FIG. 4

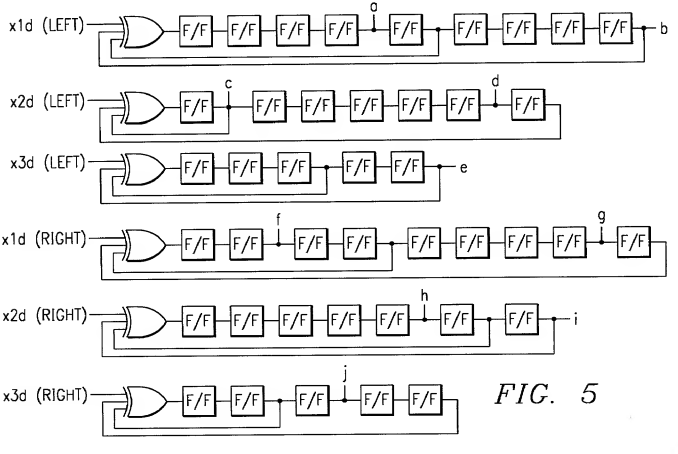

x1d (LEFT)
x2d (LEFT)
x3d (LEFT)
x1d (RIGHT)
x2d (RIGHT)
x3d (RIGHT)
F/F
a
b
c
d
e
f
g
h
i
j

FIG. 5

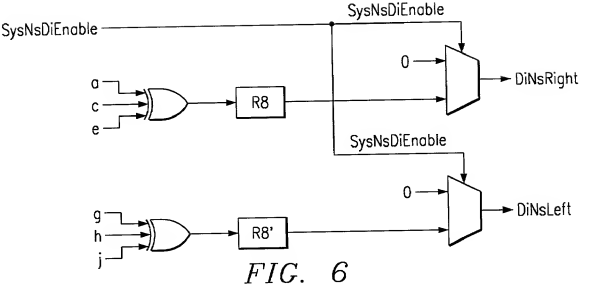



*FIG. 6*

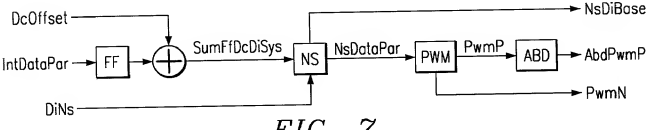



*FIG. 7*

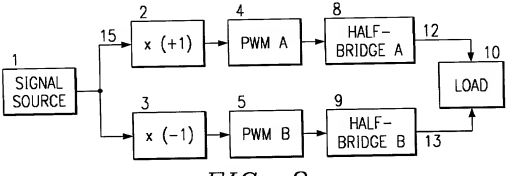



*FIG. 8*

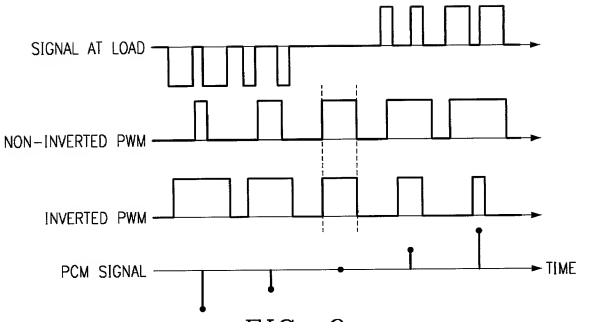



FIG. 9

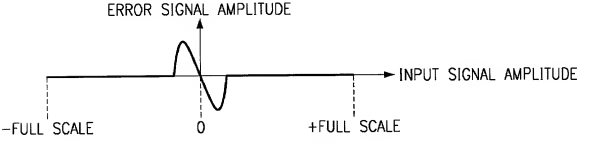



FIG. 10

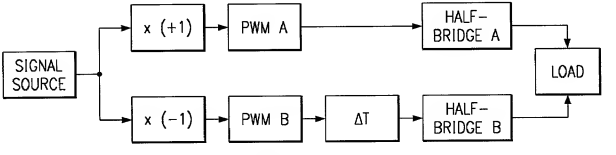



FIG. 11

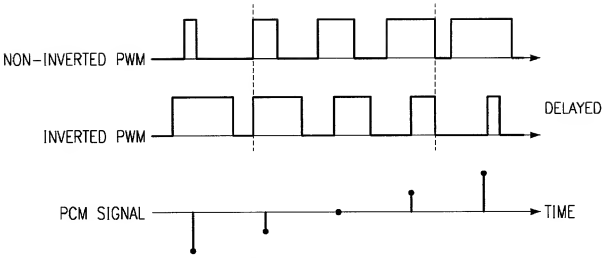



*FIG. 12*

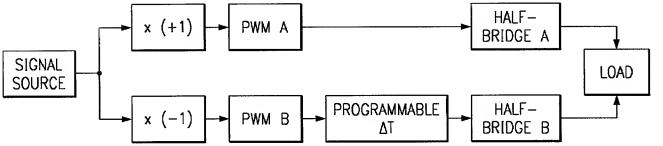



*FIG. 13*

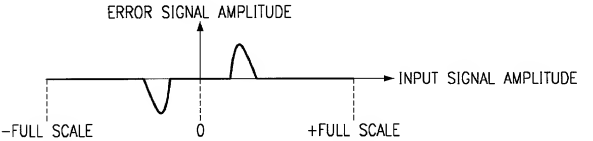



*FIG. 14*

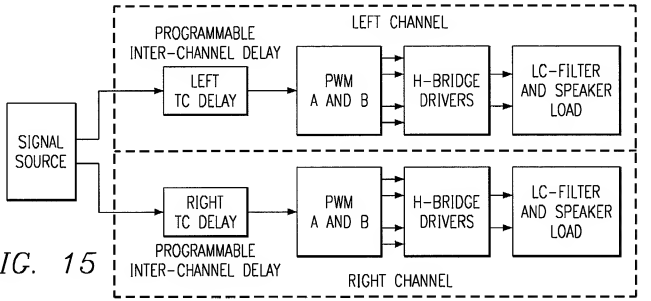

LEFT CHANNEL
PROGRAMMABLE
INTER-CHANNEL DELAY
LEFT
TC DELAY
PWM
A AND B
H-BRIDGE
DRIVERS
LC-FILTER
AND SPEAKER
LOAD
SIGNAL
SOURCE
RIGHT
TC DELAY
PWM
A AND B
H-BRIDGE
DRIVERS
LC-FILTER
AND SPEAKER
LOAD
PROGRAMMABLE
INTER-CHANNEL DELAY
RIGHT CHANNEL

FIG. 15

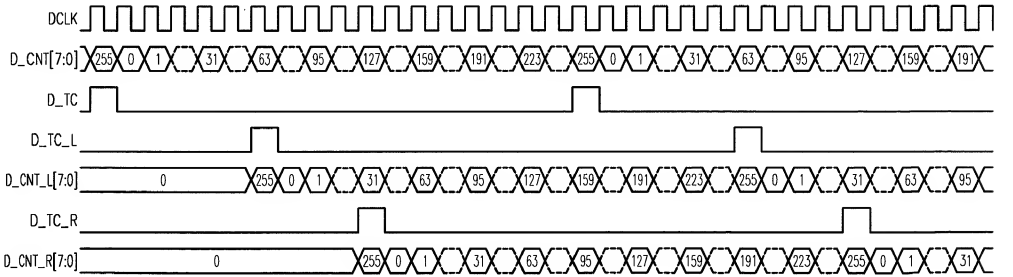

DCLK
D_CNT[7:0]
D_TC
D_TC_L
D_CNT_L[7:0]
D_TC_R
D_CNT_R[7:0]

FIG. 16

TOTE80 Z20Sh60

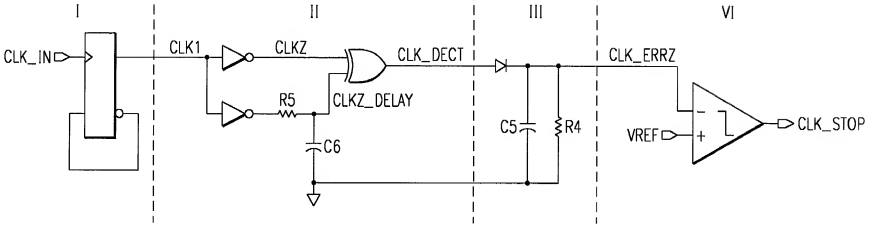
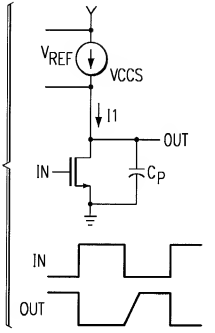



*FIG. 17*

*FIG. 18*



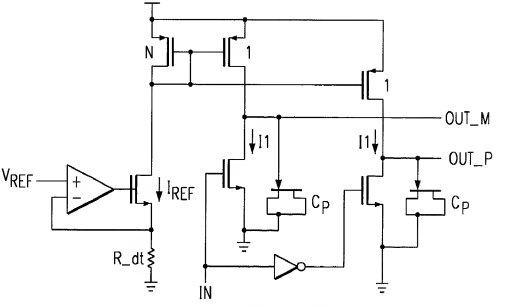




*FIG. 19*

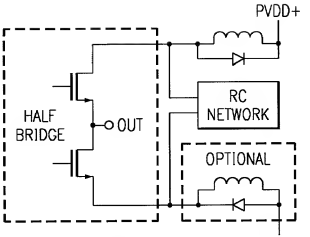



FIG. 20

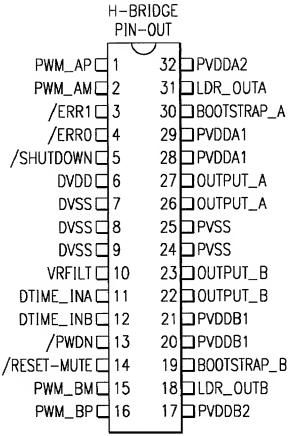



FIG. 21

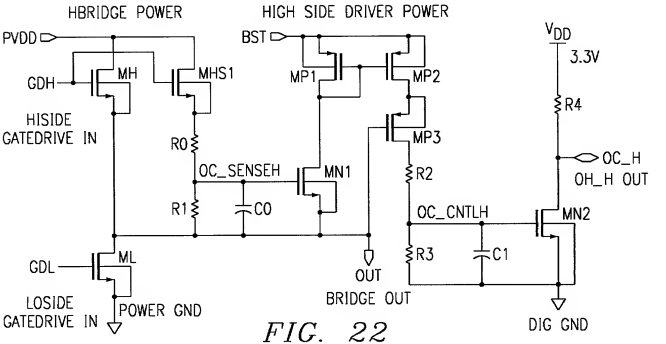



FIG. 22